

NSEP 5-WEEK DIGITAL IC DESIGN PROGRAM

The **National Semiconductor Excellence Program (NSEP)** is a 5-week intensive training initiative designed to fast-track Year 3 and Year 4 undergraduate students into high-demand roles with industry-relevant skills from the fundamentals of front-end architecture design to circuit design and the complexities of back-end physical design, verification, and layout.

Deadline: 20th June 2025

Program Structure

- Introduction to IC Design | Methodology and Verilog HDL
- Verification with VCS
- Logic Synthesis with Design Compiler
- Design for Test
- Front-end Low Power Implementation
- Static Timing Analysis with PrimeTime
- SystemVerilog TestBench
- Physical Implementation with ICC II
- Mini Project
- Presentation and Evaluation

Intake

July 2025 & September 2025

Duration

25 Days, 9.00 am - 5.00 pm

Location

PFCC, Puchong, Selangor, Malaysia.

Career Prospects

- Logic Design Engineer
- Design Verification Engineer
- Circuit Design Engineer
- Physical Design Engineer
- Software Engineer
- Design Automation Engineer
- Silicon Package Design Engineer

Entry Requirements

1. Open to:
 - a. Year 3 and Year 4 undergraduates.
 - b. Recent graduates, new hires in E&E, CS, or related fields.
2. Following the screening, there will be a mini-exam and an interview to further assess your application.
 - a. Mini-Exam: Topics include Digital Logic, Analog Circuits, General Programming, and Semiconductor Electronics.
 - b. Interview: Focused on the theme "Getting to Know You".
3. Program Deposit:
 - a. A refundable deposit of RM1,000 is required.
 - b. All deposits will be fully refunded upon successful completion of the program.

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